C L A I M S

What is claimed is:

1. A method of testing spacings in at least one pattern of openings in at least one conductive layer of a multilayered printed circuit board (PCB) to determine if said spacings meet acceptable criteria, said method comprising:

providing a multilayered PCB including an active area having at least one internal conductive layer having at least one pattern of openings therein;

providing a plurality of first patterns of apertured test pads spacedly positioned substantially along the outer periphery of said PCB externally of said active area;

providing a plurality of second patterns of apertured test pads spacedly positioned substantially adjacent said active area of said multilayered PCB and closer to said active area than said plurality of first patterns of apertured pads;

drilling a plurality of holes through said plurality of first patterns of apertured test pads to determine if each of said plurality of first patterns meet a first acceptable tolerance value;

drilling a plurality of holes through said plurality of second patterns of apertured test pads to determine if each of said plurality of second patterns meet a second acceptable tolerance value;

comparing said second acceptable tolerance value to an acceptable tolerance value assigned to said at least one pattern of openings in said active area of said PCB only if one or more of said first patterns of said apertured test pads fail to meet said first acceptable tolerance value; and

determining whether said patterns of openings in said active area meet said acceptable criteria based solely on whether the second pattern of apertured test pads nearest said pattern of openings meets said second acceptable tolerance value and not on whether others of said second patterns of apertured test pads meet said second acceptable tolerance value.

2. The method of claim 1 wherein said at least one pattern of openings in said at least one internal conductive layer are clearance openings.

3. The method of claim 3 wherein said at least one internal conductive layer is a power plane.

4. The method of claim 1 wherein said at least one pattern of openings in said at least one conductive layer are positioned within said conductive layer relative to one or more conductive lines.

5. The method of claim 4 wherein said at least one conductive layer is a signal plane.

6. The method of claim 1 wherein the number of patterns of openings in said active area of said PCB is two, said pluralities of first and second patterns of apertured pads each comprised of a first plurality of conductive pads and a second plurality of conductive pads.

7. The method of claim 6 wherein said first plurality of conductive pads in each of said pluralities of first and second patterns is associated with one of said patterns of openings in said active area and said second plurality of conductive pads in each of said pluralities of first and second patterns is associated with the other of said patterns of openings in said active area.

8. The method of claim 7 wherein each of said pluralities of first and second patterns of apertured test pads further includes an auxiliary pad, each of said first plurality of conductive pads and each of said second plurality of conductive pads being separately electrically coupled to said auxiliary pad.

9. The method of claim 8 wherein said auxiliary pad is a ground pad.

10. The method of claim 1 wherein said first acceptable tolerance value for said plurality of first patterns of apertured test pads is set to a minimum required spacing value.

11. The method of claim 1 wherein said second acceptable tolerance range for said plurality of second patterns of apertured test pads is within a range of from about 0.003 inch to about 0.008 inch.